REMARKS

This Amendment is filed in response to the Office Action dated May 21, 2004. All objections and rejections are respectfully traversed.

Claims 1-21, 28-36, and 38-66 are in the case.

Claims 1, 5, 9, 11, 19, 28, 36, 38, 40, 46, and 52-53 have been amended to better claim the invention.

Claims 54-66 have been added to better claim the invention.

At paragraph 5 of the Office Action claims 36 and 52 were rejected under 35 U.S.C. §101 as being directed to non-statutory subject matter. It is asserted that: "Electromagnetic signals are not patentable because they do not fall within one of the statutory classes of subject matter allowed by 35 U.S.C. §101."

Claim 36 is:

> 36. Electromagnetic signals propagating over a computer network comprising:
>
> ***said electromagnetic signals carrying instruction for execution on a processor for performing the method of,***
>
> defining a first register decode value that defines source operand bypassing of source operand data and a second register decode value that defines result bypassing of a result from a previous instruction executing in pipeline stages of the processor; and
>
> identifying a pipeline stage register for use as a source operand in an instruction containing the first or the second register decode value by directly addressing a source register or a result register, respectively.

Claim 52 is:

> 52. Electromagnetic signals propagating on a computer network, comprising:

said electromagnetic signals carrying instruction for the practice of the method of,

defining a register decode value that specifies source operand bypassing from a previous instruction executing in pipeline stages of the processor; and

identifying a pipeline stage register for use as a source operand in an instruction containing the register decode value by directly addressing a source register of a parallel execution unit.

Applicant respectfully points out that MPEP 2106 IV, B, 1 (c) states:

"Natural Phenomena Such as Electricity and Magnetism.

. . . However, a signal claim directed to a practical application of electromagnetic energy is statutory regardless of its transitory nature."

Applicant respectfully points out that the form of Claims 36 and 52 meet the "practical application" requirement of MPEP 2106 IV, B, 1 (c) because the claims are to: "***said electromagnetic signals carrying instruction for the practice of the method of,***" and then the method is that spelled out in the claims.

Applicant also respectfully points out that numerous editions of the MPEP, including the most recent Eighth Edition of May 2004, have been issued with the above noted section, MPEP 2106 IV, B, 1 (c), which is fully consistent with *Diamond v. Chakrabarty*, 447 U.S. 303, 206 USPQ 193 (1980).

Accordingly, Applicant respectfully urges that Claims 36 and 52 meet all statutory requirements of 35 U.S.C. §101, particularly as further set out in MPEP 2106 IV, B, 1 (c).

At paragraphs 7 and 8 of the Office Action, claim 45 was rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification. Also, at paragraph 2 of the Office Action, the drawings were objected to under 37 C.F.R. §1.83(a) for failing to show every feature of the invention specified in the claims.

Applicant respectfully urges that one skilled in the art of processor instruction sets or use with micro-opcodes and memory prefetches would inherently understand how to make or use the invention as described in Applicant's Specification (page 10). Specifically, one skilled in the art, after reading Applicant's Specification and claims would understand fully that Applicant was in possession of, and has described in an enabling manner, the use of micro-opcodes that perform memory prefetches without requiring a dedicated instruction, by realizing that the ***micro***-opcodes are contained within each instruction word, and do ***not*** require a ***dedicated*** instruction (i.e. may be ***part of*** the instruction word). Accordingly, Applicant believes that the drawing complies with al requirements of 37 C.F.R. §1.83(a), and that claim 45 is in condition for allowance.

At paragraph 9 of the Office Action, claims 36, 52, and 53 were objected to under 37 C.F.R. §1.75(c) as being of improper dependent form for failing to further limit the subject matter of a previous claim. Examiner points out that because the method steps of claims 36, 52, and 53 are directed to use with a computer, their use must inherently be embodied as electromagnetic signals or as a computer readable media. Applicant respectfully suggests that electromagnetic signals and computer readable media may be stored on (or transmitted through) some other device prior the computer executing the instructions and performing the method steps contained therein, and are therefore directed toward different subject matter. Claims 36, 52, and 53 have been amended into independent form, and are believed to be in allowable condition.

At paragraph 10 of the Office Action, claims 46-51 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claim 46 has been amended, and claims 46-51 are believed to be in allowable condition.

At paragraph 13 of the Office Action, claims 1-21, 28-36, and 38-53 were rejected under 35 U.S.C. §103 as being unpatentable over Nakada, U.S. Patent No. 5,638,526 issued June 10, 1997, in view of Asato, U.S. Patent No. 6,145,074 issued November 7, 2000. At paragraph 14 of the Office Action, the rejections from the last Office Action of June 27, 2003 were respectfully maintained and incorporated by reference.

Applicant appreciates Examiner's full response in paragraph 16 of the Office Action to Applicant's previous arguments. Applicant respectfully requests that Examiner consider Applicant's new argument below.

The present invention, as set forth in representative claim 1, comprises in part:

> 1. Apparatus for enabling an instruction to control data flow bypassing hardware within a processor of a programmable processing engine, the apparatus comprising:
>
> a pipeline of the processor, the pipeline having a plurality of stages including instruction decode, writeback, and execution stages, the execution stage having a plurality of parallel execution units; and
>
> an instruction set of the processor, the instruction set defining ***a first register decode value that defines source operand bypassing that allows source operand data to be shared among the plurality of execution units by directly addressing a source register of the plurality of execution units***, and a second register decode value that defines result bypassing that allows bypassing of a result from a previous instruction executing in pipeline stages of the processor by directly addressing a result register of the plurality of execution units.

Nakada discloses an apparatus for operand data bypassing having an operand storage register connected between an input selector and the ALU. Nakada controls the input selector by a comparator circuit (COMP), which detects a coincidence between the contents of a preceding register number in an instruction and the register number of the next instruction. When this coincidence is detected, the COMP circuit selects either a cache register (which is a copy of the operand storage register) or the result from the ALU as the input to the selector.

Asato discloses a system for selecting a standard register or previous instruction RESULT bypass as a source operand path based on a bypass specifier field in a succeeding instruction. Asato uses this bypass field as an indication of whether a register in an instruction is the RESULT of a previous instruction. An instruction in Asato will specify if the registers of an instruction are the RESULT of a previous instruction, either by the use of a bypass field, or by addressing a RESULT bypass input line from the pipeline.

Applicant respectfully urges that neither Nakada nor Asato show Applicants claims novel "***first register decode value that defines source operand bypassing that allows source operand data to be shared among the plurality of execution units by directly addressing a source register of the plurality of execution units***."

Applicant claims a system and method for directly addressing various pipeline stage registers of a plurality of execution units in a processing engine. By directly addressing the registers, the plurality of execution units can utilize source operand bypassing by, for example, sharing source operands and/or results, without having to read a register file. Applicant's claimed use of ***directly addressing*** the registers of the pipeline obviates the need for additional logic, hardware or software, to interpret a coincidence of register numbers in instructions as in Nakada. Also, by sharing the source operand among the plurality of execution units, addresses of desired data need not be repeated, whether they are internal register

addresses or external memory addresses (which can be very long). Nakada does not discuss ***directly*** addressing a source register. Asato does not discuss source operand bypassing nor sharing data among a plurality of execution units.

Stated simply, Nakada is not relevant to Applicant's claimed invention because Nakada uses a comparator circuit rather than Applicant's novel values in Applicant's instruction set. Further, Asato has no disclosure whatever concerning Applicant's claimed source operand bypassing. Accordingly, Applicant's claims are believed to be in condition for allowance.

Applicant respectfully urges that the Nakada patent and the Asato patent, either taken singly or in any combination are legally insufficient to render the presently claimed invention obvious under 35 U.S.C. §103 or from anticipating the claimed invention under 35 U.S.C §102 because of the absence in each of the cited patents of Applicant's claimed novel "***first register decode value that defines source operand bypassing that allows source operand data to be shared among the plurality of execution units by directly addressing a source register of the plurality of execution units***."

Further, Applicant presents new claim 64 as follows:

64. An apparatus for enabling an instruction to control data flow bypassing hardware within a processor of a programmable processing engine, the apparatus comprising:

a pipeline of the processor, the pipeline having a plurality of stages including instruction decode, writeback, and execution stages, the execution stage having a plurality of parallel execution units; and

an instruction set of the processor, the instruction set defining a register decode value that specifies source operand bypassing.

Applicant respectfully urges that neither Nakada nor Asato disclose ***an instruction set defining a register decode value that specifies source operand bypassing***. To the contrary, Nakada only uses a hardware comparator circuit for determining a bypass, and Asato merely addresses result operand bypassing. Accordingly, Applicant believes that the claims are in condition for allowance.

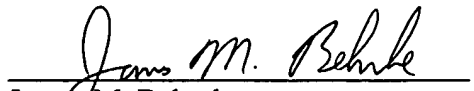
All independent claims are believed to be in condition for allowance.

All dependent claims are believed to be dependent from allowable independent claims, and therefore in condition for allowance.

Favorable action is respectfully solicited.

Please charge any additional fee occasioned by this paper to our Deposit Account No. 03-1237.

Respectfully submitted,



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